

Abstract

Coherency techniques for suspending execution of a thread until a specified memory access occurs. In one embodiment, a processor includes a cache, execution logic
5 to execute an instruction having an operand indicating a monitor address and a bus controller. In one embodiment, the bus controller is to assert a preventative signal in response to receiving a memory access attempting to gain sufficient ownership of a cache line associated with said monitor address to allow modification of said cache line without generation of another transaction indicative of the modification. In another embodiment,
10 the bus controller is to generate a bus cycle in response to the instruction to eliminate any ownership of the cache line by another processor that would allow a modification of the cache line without generation of another memory access indicative of the modification.